Abstract

A fractional clock divider system and method is provided. The clock divider is configured to provide an output clock signal in response to an input clock signal. The frequency of the output clock signal may be an integral or fractional division of the input clock signal. The output frequency is equal to: (ref_freq * 2) / mul, where ref_freq is the frequency of the input clock signal, and mul is a selected integer that is greater than one. The positive and negative edges of the input clock are counted to provide a positive count and a negative count respectively. A table is configured to store preselected reference values. A logic circuit is configured to control the output clock signal such that an appropriate clock transition occurs in the output clock signal when the positive and negative count reach the corresponding preselected reference values.